REMARKS

In the Office Action of May 8, 2001, Examiner Dang suggests that Claims 1 through 15 are drawn to a first invention (Group I), while Claims 16 through 20 are drawn to a second invention (Group II). Consequently, Examiner Dang has required Applicants to elect a single species.

I. Election of Species

Applicants hereby elect Group II for prosecution in the instant application. In so doing, Applicants reserve all rights to their Group I invention, as reflected in their originally filed Claims 1 through 15.

II. Summary and Conclusion

Applicants believe that a full and complete response has been made to Examiner Dang's Office Action. Thus, in view of the hereinabove remarks, Applicants respectfully requests reconsideration and allowance of their patent application and its claims.

To that end, if the Examiner feels that a conference might expedite the prosecution of this case, he is cordially invited to call the undersigned.

Respectfully submitted,

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COMPUTER RED-LINED VERSION

A METHOD OF FABRICATING A HETEROJUNCTION BIPOLAR TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

Related subject matter is disclosed in co-pending, commonly assigned, U.S. Patent applications Serial Number 09/396,035, filed on September 15, 1999, entitled "Alignment Techniques For Epitaxial Growth Processes."

FIELD OF THE INVENTION

The present invention relates to semiconductors, generally, and more particularly to a method of fabricating a heterostructure device, such as a Double Heterojunction Bipolar Transistor ("DHBT").

BACKGROUND OF THE INVENTION

III-V bipolar transistors are three terminal devices having three regions of alternating conductivity type, referred to as the emitter, base, and collector, constructed from III and V semiconductor compounds. One class of III-V bipolar transistors gaining notoriety is heterostructure devices - heterojunction bipolar transistors ("HBTs") and double heterojunction bipolar transistors ("DHBTs"). HBT and DHBTs include a junction between materials of differing composition, such as InGaAs and InP. In such an exemplary device structure, the InGaAs material has several known distinct properties from the InP material. These characteristics are detailed in depth in various references, including Sze, Physics of Semiconductor Device, Wiley-Interscience, 1969, pp. 17-24 and 140-146 (hereinafter "Sze"), Williams, Gallium Arsenide Processing Techniques, Artech House, Inc., 1984, pp. 17-35 and 79-82 (hereinafter "Williams"), and Streetman, Solid State Electronic Devices, Prentice-Hall, Inc., 1980, pp. 52-96, 395-399, and 424-428 (hereinafter "Streetman") which are hereby incorporated by reference.

Various methods of fabricating III-V DHBT devices are known in the art. Referring to **FIG. 1**, a multi-layer structure **5** is shown prior to undergoing the